(PCN item # 1) Serial Ports-Enable and Three-State comparison for BF538/ BF538F Rev D & Rev E data sheets

Rev D product data sheet:

Table 33. Serial Ports—Enable and Three-State

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DTENE}	Data Enable Delay from External TSCLKx[1]	0		ns
t_{DDTTE}	Data Disable Delay from External TSCLKx[1]		10.0	ns
t_{DTENI}	Data Enable Delay from Internal TSCLKx[1]	–2.0		ns
t_{DDTTI}	Data Disable Delay from Internal TSCLKx[1]		3.0	ns

[1] Referenced to drive edge.

Rev E product data sheet:

Table 33. Serial Ports—Enable and Three-State

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DTENE}	Data Enable Delay from External TSCLKx[1]	0		ns
t_{DDTTE}	Data Disable Delay from External TSCLKx[1,2,3]		10	ns
t_{DTENI}	Data Enable Delay from Internal TSCLKx[1]	–2		ns
t_{DDTTI}	Data Disable Delay from Internal TSCLKx[1,2,3]		3	ns

[1] Referenced to drive edge.
[2] Applicable to multichannel mode only.
[3] TSCLKx is tied to RSCLKx.

ANALOG DEVICES

Other Changes for Rev E data sheet (PCN item #'s 2 & 3)

- **(PCN item #2):**
  - **Added new footnote #3 to Operating Conditions Table:**
  - *When VDDEXT < 2.70 V, on-chip voltage regulation is not supported*

- **(PCN item #3):**
  - **Added new Table #38 for Timer Clock Timing**

Table 38. Timer Clock Timing

Parameter		Min	Max	Unit
Switching Characteristic				
t_{TODP}	Timer Output Update Delay After PPI_CLK High		12	ns

ANALOG DEVICES

(PCN item #'s 4 & 5) Timer Cycle Timing comparison for BF538/ BF538F Rev D & Rev E data sheets

Rev D product data sheet:

Table 38. Timer Cycle Timing

Parameter		Min	Max	Unit
Timing Characteristics				
t_{WL}	Timer Pulse Width Input Low[1] (Measured in SCLK Cycles)	1		SCLK
t_{WH}	Timer Pulse Width Input High[1] (Measured in SCLK Cycles)	1		SCLK
Switching Characteristic				
t_{HTO}	Timer Pulsewidth Output (measured in SCLK Cycles)	1	$(2^{32} - 1)$	SCLK

[1] The minimum pulse widths apply for TMRx input pins in width capture and external clock modes. They also apply to the PF1 or PPI_CLK input pins in PWM output mode.

Rev E product data sheet:

Table 39. Timer Cycle Timing

Parameter		Min	Max	Unit
Timing Characteristics				
t_{WL}	Timer Pulse Width Input Low[1]	$1 \times t_{SCLK}$		ns
t_{WH}	Timer Pulse Width Input High[1]	$1 \times t_{SCLK}$		ns
t_{TIS}	Timer Input Setup Time Before CLKOUT Low[2]	6.5		ns
t_{TIH}	Timer Input Hold Time After CLKOUT Low[2]	–1		ns
Switching Characteristics				
t_{HTO}	Timer Pulse Width Output	$1 \times t_{SCLK}$	$(2^{32} - 1) \times t_{SCLK}$	ns
t_{TOD}	Timer Output Delay After CLKOUT High		6	ns

[1] The minimum pulse widths apply for TMRx signals in width capture and external clock modes.
[2] Either a valid setup and hold time or a valid pulse width is sufficient. There is no need to resynchronize timer flag inputs.

ANALOG DEVICES